Product Reliability Qualification Strategy & Report PPAP

Quad source TJA1028TK/5V0/10, TJA1028TK/5V0/20, TJA1042TK/3, TJA1049TK, TJA1049TK/3, TJA1051TK/3

3.0 — August 25, 2022

Document information

Info	Content
Author / Department	Tino Heijmen / Global Quality
Business Line	BL Advanced Analog
Product Line / Location	PL In Vehicle Networking / Nijmegen
Market	Automotive
Document ID	DOC-271840

Revision	Date	Description	Author
1.0	September 9, 2020	Initial revision.	Tino Heijmen
2.0	October 20, 2021	Results added for TJA1042TK/3	Tino Heijmen
3.0	August 25, 2022	Results added for TJA1051TK/3	Tino Heijmen

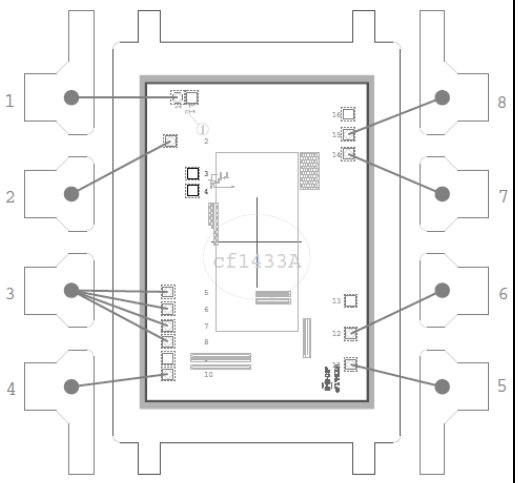
Contents

1. Summary

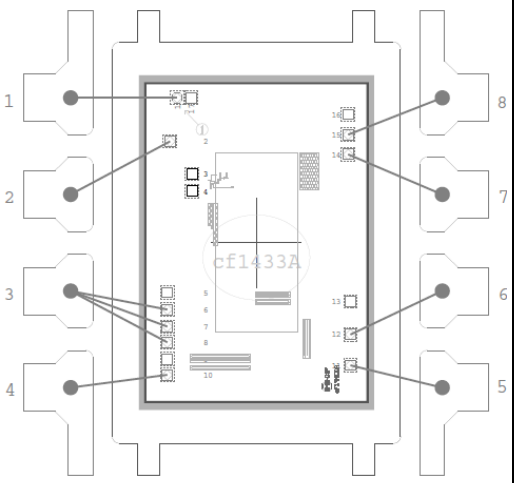
The current report describes the failure-mechanism based stress-test qualification of second-source assembly release of the product types listed in Table 1. All products in scope are assembled in HVSON8 (SOT782-1) and are assembly second-sourced from ATBK to ASEN[1]. In addition, the released product types are front-end dual-sourced in wafer-fabrication process (A-BCD3) from ICN8 to SSMC. Section 3.12 describes the wire-diameter change from 20 to 18 µm in ATBK for TJA1028TK/5V0/XX (XX = 10 or 20), TJA1042TK/3, and TJA1051TK/3 manufactured either in ICN8 or SSMC. The extensions "/10" and "/20" in the TJA1028 product name are related to the supported baud rate, see the product datasheet. The difference between the "low-slope" TJA1028TK/5V0/10 and the "normal-slope" TJA1028TK/5V0/ is determined by the wire bond-out, see Figure 1.

Table 1. Product types qualified with the results reported in the current report.

Type name	Grade	Ambient Operating Temperature Range
TJA1028TK/5V0/XX[2]	1	-40 °C to +125 °C
TJA1042TK/3	1	-40 °C to +125 °C
TJA1049TK	1	-40 °C to +125 °C
TJA1049TK/3	1	-40 °C to +125 °C
TJA1051TK/3	1	-40 °C to +125 °C



TJA1028TK/5V0/10



TJA1028TK/5V0/20

Figure 1. Bond-out of TJA1028TK/5V0 product versions.

The difference between TJA1049TK and TJA1049TK/3 is also determined by the wire bond-out, see Figure 2.

[1] Currently, ASEN is named ATX-SZ.

[2] XX = 10 or 20.

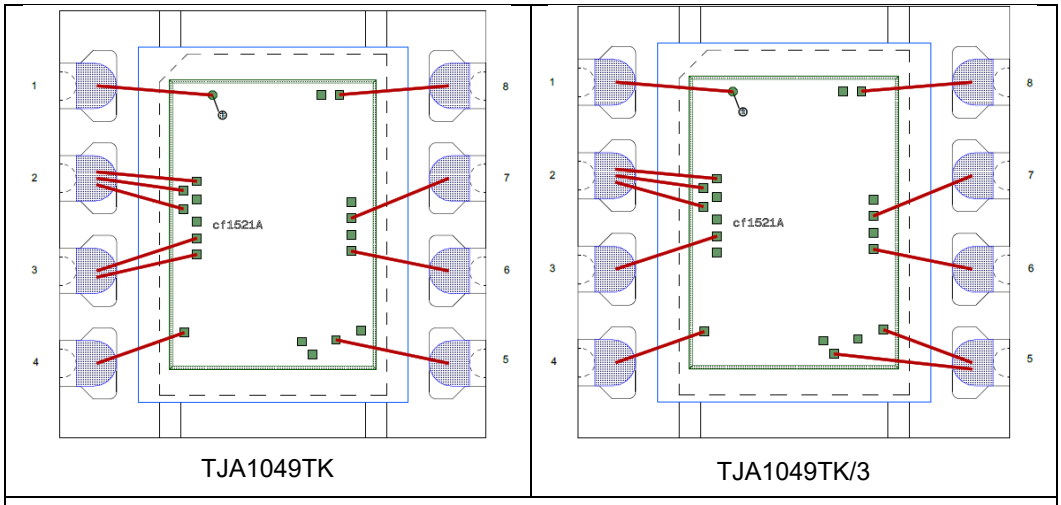


Figure 2. Bond-out of TJA1049TK and TJA1049TK/3 product versions.

The qualification strategy has been defined according to NXP's internal reliability qualification policy and customer requirements. The strategy has been compliant with the automotive standard AEC Q100 Revision G.

Where possible, generic data have been used to satisfy qualification requirements. Test samples have been representative of the applied wafer-fab and assembly processes. All qualification devices were produced on tooling and processes at the manufacturing sites that are used to support part deliveries at production volumes.

The qualification program document in the current report has been completed successfully. As a result, the product types have been AEC Q100 qualified and released.

2. Qualification test results

2.1 Qualification material

For reliability qualification testing of TJA1028TK, the “normal-slope” version TJA1028TK/5V0/20 was used. “Low-slope” version TJA1028TK/5V0/10 is structural similar to the normal-slope version for all reported tests.

Table 2. Qualification lots.

	New stress test results – generated on the product type(s) to be qualified								
Qual lot ID	Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	Lot 6	Lot 7	Lot 8	Lot 9
Product name	TJA1028TK	TJA1028TK	TJA1028TK	TJA1049TK/3	TJA1028TK	TJA1028TK	TJA1049TK/3	TJA1028TK	TJA1028TK
Design version	tf1433A	tf1433A	tf1433A	tf1521A	cf1433A	cf1433A	tcf1521A	tf1433A	cf1433A
Package	SOT782-1	SOT782-1	SOT782-1	SOT782-1	SOT782-1	SOT782-1	SOT782-1	SOT782-1	SOT782-1
Wafer fab site	SSMC	SSMC	SSMC	SSMC	ICN8	ICN8	ICN8	SSMC	ICN8
Wafer batch ID	SNW093.1	N/A	SNW093.1	SKG962.1	CHX810	CWT758	CWW4632	SNW093.104	CWT758
Wafer slice nr	6	N/A	8	15	1	2	22	4	6
Assembly site	ASEN	ASEN	ASEN	ASEN	ASEN	ASEN	ASEN	ATBK	ATBK
Assy date code	N0S939694000	N/A	N0S944EWT200	N0S944EVW200	N0S945418100	N0S939697000	N0S944EU6100	N0S931CAN100	N0S930DKC110
Used for test(s)	MSLA / HAST / TC / HTSL / CDM / ConAna	BL-TC	HAST / TC / HTSL	CDM / ConAna	MSLA / HAST / TC / HTSL / ConAna	CDM	CDM / ConAna	CDM / ConAna	CDM / ConAna

	New stress test results – generated on the product type(s) to be qualified								
Qual lot ID	Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	Lot 6	Lot 7	Lot 8	Lot 9
Product name	TJA1028TK	TJA1028TK	TJA1028TK	TJA1049TK/3	TJA1028TK	TJA1028TK	TJA1049TK/3	TJA1028TK	TJA1028TK
Design version	tf1433A	tf1433A	tf1433A	tf1521A	cf1433A	cf1433A	tcf1521A	tf1433A	cf1433A
Package	SOT782-1	SOT782-1	SOT782-1	SOT782-1	SOT782-1	SOT782-1	SOT782-1	SOT782-1	SOT782-1
Wafer fab site	SSMC	SSMC	SSMC	SSMC	ICN8	ICN8	ICN8	SSMC	ICN8
Wafer batch ID	SNW093.1	N/A	SNW093.1	SKG962.1	CHX810	CWT758	CWW4632	SNW093.104	CWT758
Wafer slice nr	6	N/A	8	15	1	2	22	4	6
Assembly site	ASEN	ASEN	ASEN	ASEN	ASEN	ASEN	ASEN	ATBK	ATBK
Assy date code	N0S939694000	N/A	N0S944EWT200	N0S944EVW200	N0S945418100	N0S939697000	N0S944EU6100	N0S931CAN100	N0S930DKC110
Used for test(s)	MSLA / HAST / TC / HTSL / CDM / ConAna	BL-TC	HAST / TC / HTSL	CDM / ConAna	MSLA / HAST / TC / HTSL / ConAna	CDM	CDM / ConAna	CDM / ConAna	CDM / ConAna

	Generic data – previously generated on the current product type(s)							
Qual lot ID	Lot 18	Lot 19	Lot 20	Lot 21	Lot 22	Lot 23	Lot 24	Lot 25
Product name	TJA1028	TJA1028	TJA1028	TJA1049	TJA1028	TJA1028	TJA1028TK	TJA1028TK
Package	SO8	SO8	SO8	SO8	SO8	SO8	HSVON8	HSVON8
Wafer fab site	ICN8	ICN8	ICN8	ICN8	ICN8	SSMC	ICN8	SSMC
Wafer batch ID	CS4074	CS4580	CS5276	CR9492	CS4580	S98789.1	CT0240	S98789.1
Wafer slice nr				02	01, 02			
Assembly site	ATBK	ATBK	ATBK	ATBK	ATBK	ATBK	ATBK	ATBK
Used for test(s)	HTOL	HTOL	HTOL	HTOL	HBM	HBM	CDM	MSLA / HAST / TC / HTSL / CDM / ConAna

	Generic data – previously generated on the current product type(s)							
Qual lot ID	Lot 26	Lot 27	Lot 28	Lot 29	Lot 30	Lot 31	Lot 32	Lot 33
Product name	TJA1049	TJA1049	TJA1049/3	TJA1049/3	TJA1049TK	TJA1049TK	TJA1049TK/3	TJA1049TK/3
Package	SO8	SO8	SO8	SO8	HVSON8	HVSON8	HVSON8	HVSON8
Wafer fab site	ICN8	SSMC	ICN8	SSMC	ICN8	SSMC	ICN8	SSMC
Wafer batch ID	CKX813	S64678.1	CW5734	S64678.1	CKX813	S64678.1	CW5734	S64678.1
Wafer slice nr								
Assembly site	ATBK	ATBK	ATBK	ATBK	ATBK	ATBK	ATBK	ATBK
Used for test(s)	HBM	HBM	HBM	HBM	CDM	MSLA / HAST / TC / HTSL / CDM / ConAna	CDM	CDM

	Generic data – previously generated on other product types											
Qual lot ID	Lot 34	Lot 34	Lot 35	Lot 36	Lot 37	Lot 38	Lot 39	Lot 40	Lot 41	Lot 42	Lot 43	Lot 44
Product name	N/A	TJA1042	TJA1044	UJA1078	UJA1078	TJA1051	UJA1078A	UJA1078A	UJA1078A	TJA1059TK	TJA1059TK	TJA1059TK
Design version												
Package	HVSON8	SO8	SO8	HTSSOP32	HTSSOP32	SO8	HTSSOP32	HTSSOP32	HTSSOP32	HVSON14	HVSON14	HVSON14
Wafer fab site	N/A	ICN8	ICN8	ICN8	ICN8	ICN8	SSMC	SSMC	SSMC	ICN8	ICN8	ICN8
Wafer batch ID	N/A	CK0984	CAY862	CR1469	CR1748	CM3461	S98633	S98787	S98728	CYS434	CYS431	CYS323
Wafer slice nr	N/A	02	08	05	01, 03	05	2	1	2			
Assembly site	ATBK	ATBK	ATBK	ATBK	ATBK	ATBK	ATBK	ATBK	ATBK	ATBK	ATBK	ATBK
Assy date code										2034	2035	2036
Used for test(s)	DIMS	HTOL	HTOL	ELFR	ELFR	ELFR	HTOL, ELFR	HTOL, ELFR	HTOL, ELFR	UHAST	UHAST	UHAST

2.2 Stress test results

Table 3. Test group A – Accelerated environmental stress tests.

						New stress test results – generated on the product type(s) to be qualified			Generic data – previously generated on the current product type(s)	Generic data – previously generated on other product types			
Q100 Test #	**Test abbr.**	**Stress test conditions**	**Read-points**	**ATE temperatures**	**Required total # units**	**Lot 1**	**Lot 3**	**Lot 5**	**Lot 25**	**Lot 42**	**Lot 43**	**Lot 44**	**Comments**
	MSLA	Moisture Sensitivity Level Assessment / Verification			1 x 14	MSL L1		MSL L1	MSL L1				
A1 + A2	**PCON L.1 + HAST**	Highly Accelerated Stress Test @ 130 °C / 85% RH Vstress = 28 V	0 Hrs.	R, H	3 x 77	0 / 77	0 / 77	0 / 77	0 / 77				
			PCON			0 / 77	0 / 77	0 / 77	0 / 77				
			96 hrs			0 / 77	0 / 77	0 / 77	0 / 77				
			192 hrs			0 / 77	0 / 77	0 / 77	0 / 77				
			384 hrs			0 / 77							
			CSAM 0 hrs		3 x 14	0 / 14	0 / 14	2 / 14 [a]					
			CSAM PCON			0 / 14	0 / 14	0 / 14					
A1 + A3	**PCON L1 + UHAST**	Unbiased Highly Accelerated Stress Test @ 130 °C / 85% RH	0 Hrs.	R	3 x 77					0 / 77	0 / 77	0 / 77	UHAST is also covered by HAST.
			PCON							0 / 77	0 / 77	0 / 77	
			96 hrs							0 / 77	0 / 77	0 / 77	
			192 hrs										
			384 hrs										
A1 + A4	**PCON L.1 + TC**	Temperature Cycling @ -65 to +150 °C with WBP (#C2) after TC	0 Hrs.	R, H	3 x 77	0 / 77	0 / 77	0 / 77	0 / 77				
			PCON			0 / 77	0 / 77	0 / 77	0 / 77				
			500 cycles			0 / 77	0 / 77	0 / 77	0 / 77				
			1000 cycles			0 / 77	0 / 77	0 / 77	0 / 77				
			1500 cycles			0 / 77			0 / 77				
			CSAM 0 hrs		3 x 14	0 / 14	0 / 14	0 / 14	0 / 14				
			CSAM PCON			0 / 14	0 / 14	0 / 14	0 / 14				
			WBP 500 cycles		3 x 5	0 / 5	0 / 5	0 / 5	0 / 5				
A5	**PCON L1 + PTC**	Power Temperature Cycling @ -40 to +125 °C	0 Hrs	R, H	1 x 45								PTC is not required as maximum rated power < 1 Watt and delta Tj < 40 °C.
			CSAM										
			PCON										
			CSAM										
			1000 cycles										
			2000 cycles										
A6	**HTSL**	High Temperature Storage Life @ 175 °C	0 Hrs	R, H	3 x 77	0 / 77	0 / 77	0 / 77	0 / 77				
			500 hrs			0 / 77	0 / 77	0 / 77	0 / 77				
			1000 hrs			0 / 77	0 / 77	0 / 77	0 / 77				

Notes:

a Lead delamination was observed after pre-conditioning. This problem has been addressed and resolved, see section 2.3.2.

Table 4. Test group B – Accelerated lifetime simulation tests.

						Generic data – previously generated on the current product type(s)						Generic data – previously generated on other product types						
Q100 Test #	**Test abbr.**	**Stress test conditions**	**Read-points**	**ATE temperature**	**Required total # units**	**Lot 18**	**Lot 19**	**Lot 20**	**Lot 21**	**Lot 34**	**Lot 35**	**Lot 36**	**Lot 37**	**Lot 38**	**Lot 39**	**Lot 40**	**Lot 41**	**Comments**
B1	**HTOL**	High Temperature Operating Life (Intrinsic Life) @ Tj ≥ 150 °C Grade 1	0 Hrs.	R, C, H	3 x 77	0 / 77	0 / 77	0 / 77	0 / 77	0 / 77	0 / 77				0 / 77	0 / 77	0 / 77	
			168 Hrs			0 / 77	0 / 77	0 / 77	0 / 77	0 / 77	0 / 77				0 / 77	0 / 77	0 / 77	
			1008 Hrs			0 / 77	0 / 77	0 / 77	0 / 77	0 / 77	0 / 77				0 / 77	0 / 77	0 / 77	
			2016 Hrs			0 / 77				0 / 77	0 / 77				0 / 77	0 / 77		
			3024 Hrs							0 / 77	0 / 77				0 / 77			
			4032 Hrs							0 / 77	0 / 77				0 / 77			
B2	**ELFR**	Early Life Failure Rate @ Tj ≥ 150 °C Grade 1	0 Hrs.	R, H	3 x 800							0 / 800	0 / 800	0 / 800	0 / 800	0 / 800	0 / 800	
			48 Hrs									0 / 800	0 / 800	0 / 800	0 / 800	0 / 800	0 / 800	
B3	**EDR**	Non-Volatile Memory Endurance, Data Retention, and Operational Life: Erase / Program Endurance @ Tj = 85 °C	# cycles according to device specification		1 x 77													Not applicable, because product does not include NVM.
B3	**EDR**	Non-Volatile Memory Endurance, Data Retention, and Operational Life: Data Retention @ Tj = 150 °C Unbiased	1000 Hrs		1 x 77													Not applicable, because product does not include NVM.

Table 5. Test group C – Package assembly integrity tests

					New stress test results – generated on the product type(s) to be qualified														Generic data – previously generated on the current product type(s)		Generic data – previously generated on other product types	
Q100 Test #	**Test abbr.**	**Stress test conditions**	**Read-points**	**Required total # units**	**Lot 1**	**Lot 3**	**Lot 4**	**Lot 5**	**Lot 7**	**Lot 8**	**Lot 9**	**Lot 10**	**Lot 11**	**Lot 12**	**Lot 13**	**Lot 14**	**Lot 15**	**Lot 16**	**Lot 17**	**Lot 25**	**Lot 31**	**Lot 34**	**Comments**
C1	**WBS**	Wire Bond Shear		30 bonds from 5 devices	Pass		Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass		See appendix for detailed test results.
C2	**WBP**	Wire Bond Pull Condition C: single bond	0 Hrs.	30 bonds from 5 devices	Pass		Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass		See appendix for detailed test results.
			TC 500 cls		Pass	Pass		Pass												Pass			
C3	**SD**	Solderability	Dry Bake	15	Pass																		See appendix for detailed test results.
			Steam Aging		Pass																		
C4	**PD**	Physical Dimensions		10	Pass		Pass	Pass		Pass	Pass											Pass	See dimensions report for detailed results.
C5	**SBS**	Solder Ball Shear		5 balls from 10 devices																			Not applicable, because device is not solder-ball surface-mount packaged (BGA).
C6	**LI**	Lead Integrity		10 leads from each of 5 parts																			Not applicable, because device is surface mount.
	CSAM	Scanning Acoustic Microscopy inspection		22	Pass		Pass	Pass		Pass	Pass												See appendix for detailed test results.
	Xray	Xray inspection		10	Pass		Pass		Pass	Pass		Pass		Pass		Pass		Pass					See appendix for detailed test results.

Table 6. Test group D – Die fabrication reliability tests

		ICN8		SSMC	
Q100 Test #	**Failure mechanism**	**Sample size**	**Result**	**Sample size**	**Result**
D1	**Electromigration**	**3B, 15 lines per condition**	Pass	**3B, 15 lines per condition**	Pass
D2	**Time Dependent Dielectric Breakdown**	**3B x >10S**	Pass	**3B x >10S**	Pass
D3	**Hot Carrier Injection**	**3B x 15S**	Pass	**3B x 9S**	Pass
D4	**Negative Bias Temperature Instability**	**3B x 15S**	Pass	**3B x 3S**	Pass
D5	**Stress Migration**	**> 1 cm**	Pass	**> 1 cm**	Pass

Table 7. Test group E – Electrical verification tests.

					New stress test results – generated on the product type(s) to be qualified															Generic data – previously generated on the current product type(s)																Generic data – previously generated on other product types								
Q100 Test #	**Test abbr.**	**Stress test conditions**	**Required total # units**	**ATE temp.**	**Lot 1**	**Lot 3**	**Lot 4**	**Lot 5**	**Lot 6**	**Lot 7**	**Lot 8**	**Lot 9**	**Lot 10**	**Lot 11**	**Lot 12**	**Lot 13**	**Lot 14**	**Lot 15**	**Lot 16**	**Lot 17**	**Lot 18**	**Lot 19**	**Lot 20**	**Lot 21**	**Lot 22**	**Lot 23**	**Lot 24**	**Lot 25**	**Lot 26**	**Lot 27**	**Lot 28**	**Lot 29**	**Lot 30**	**Lot 31**	**Lot 32**	**Lot 33**	**Lot 34**	**Lot 35**	**Lot 36**	**Lot 37**	**Lot 38**	**Lot 39**	**Lot 40**	**Comments**
E1	**TEST**	Pre- and Post-Stress Function/Parameter			Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Devices tested at every readpoint in compliance with AEC Q100-007. Includes parameter shift analysis after ELFR (2T), HTOL (3T), HBM (2T), and CDM (2T). No significant shifts have been observed.
E2	**HBM / MM**	Electrostatic Discharge Human Body Model / Machine Model		R, H																				Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass												See PPAP ESD report for detailed results.
E3	**CDM**	Electrostatic Discharge Charged Device Model		R, H	Pass		Pass		Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass								Pass				Pass	Pass	Pass	Pass								See PPAP ESD report for detailed results.
E4	**LU**	Latch-Up	1 x 6	R, H																																							Not applicable, because device is fabricated in latch-up immune SOI process.
E5	**ED**	Electrical Distributions	3 x 30	R, C, H																																							See PPAP ED report for detailed results.
E6	**FG**	Fault Grading																																										See PPAP Certificate of Design, Construction, and Qualification (CDCQ) for stuck-at fault coverage. The acceptance criteria from AEC Q100-007 are met for all devices submitted for qualification.
E7	**CHAR**	Characterization																																										Datasheet guaranteed by wafer test and final test. See PPAP ED report for detailed results. The acceptance criteria from AEC Q003 are met.
E8	**GL**	Gate Leakage	1 x 6	R																																								For information only.
E9	**EMC**	Electromagnetic Compatibility	1 x 1																																								See PPAP EMC report for detailed results.
E10	**SC**	Short Circuit Characterization	3 x 10																																									Not applicable, because is not a smart power device as defined in AEC Q100-012.
E11	**SER**	Soft Error Rate	1 x 3																																									Not applicable, because device does not contain SRAM and is not released for ISO26262 functional safety application.

Sample sizes and acceptance criteria for Part Average Testing (PAT, AEC Q100 test #F1) are determined in accordance with AEC Q001. Sample sizes and acceptance criteria for Statistical Bin/Yield Analysis (SBA, AEC Q100 test #F2) are determined in accordance with AEC Q002.

AEC Q100 test group F on Cavity Package Integrity testing is not applicable, because the device is not assembled in a hermetic package..

Table 8. Test group Board-Level Reliability test.

			New stress test results – generated on the product type(s) to be qualified	
Test abbr.	**Stress test**	**Required total # units**	**Lot 2**	**Comments**
BL TC	Board Level Temperature Cycling -40 to +125 C on daisy-chain component	1 x 30	Pass. First fail at 3158 cls. Eta-value at 4285 cls.[a]	No completed crack in bulk of solder joint observed near both PCB and component side after 1000 and 2000 cls.

Notes:

a Eta is the scale parameter in the two-parameter Weibull distribution and represents 63.2% cumulative failure rate.

2.3 Failure analysis and corrective actions

2.3.1 Cratering after WBS

Cratering was observed after wire-bond shear (WBS) testing during construction analysis of qualification lot 5. No cratering was observed after WBS testing of lots 1, 3, 7, 8, and 9. Wire-bond shear test results of lot 5 show a normal distribution, within specification, see section 3.5. An 8D investigation showed that the root cause was an abnormal ultra-sonic generator (USG) impedance. As a corrective action, the transducer of the wire-bonder was replaced, resulting in a stable USG performance. Furthermore, a system based on an out-of-control plan (OCAP) was built to monitor the USG performance and to replace the transducer. Also, the spec to check cratering during ball-shear test after wire-bonding was updated. Additionally, actions were taken to prevent reoccurrence, such as updating the FMEA. The first 10 assembled production lots were checked for cratering during ball-shear test, applying a sample size of 5 units per lot. No cratering was observed.

2.3.2 Lead delamination after PCON

After pre-conditioning before HAST of lot 5, CSAM analysis showed lead delamination on 2 samples out of 14, see Table 3. No delamination was observed on lots 1 and 3. Also, no delamination was found after PCON for lot 5 samples for TC. Visual inspection showed plating peel-off on the leads. During an 8D investigation, the lead delamination was not observed on other samples, even not after PreCon was performed on 77 samples of both the affected lot and a control lot. Checks of the process mapping and process variation did not show any abnormalities. The plating peel-off was discussed with the lead-frame supplier, but that did not reveal any abnormalities or give an indication of the root cause. Also other investigations did not reveal a potential root cause. As corrective actions, the following measures have been defined:

- The sample size for the plating peel-off test at incoming inspection was increased for the first 20 batches. No plating peel-off was observed.
- 100% automated optical inspection (AOI) was installed for the first 10 assembled production lots. No abnormalities were observed.
- CSAM analysis was performed for the first 10 assembled production lots, to check for lead delamination. No delamination was observed.
- PCON followed by CSAM analysis was performed for the first 10 assembled production lots. No delamination was observed, neither at 0 hrs nor after PCON.

The results from these measures all passed the criteria. Therefore, the lead delamination, observed on only two devices during qualification, was a one-time incident.

2.4 Conclusions

TJA1028TK, TJA1042TK/3, TJA1049TK, TJA1049TK/3, and TJA1051TK/3 in HVSON8 (SOT782-1), manufactured in ICN8 or in SSMC wafer-fab and assembled in ATBK or ASEN, with 18-μm Au-wire, can be released for mass production. The qualification results comply with NXP's internal requirements and AEC-Q100 Rev G, Grade 1 [1].

2.5 References

1. Failure mechanism based stress test qualification for integrated circuits, AEC-Q100 – Rev-G, May 17, 2007.
2. Pb-free test requirements, AEC – Q005 – Rev-A, June 1, 2010.
3. Dimensional Results (part of PPAP).
4. ESD Report (part of PPAP).
5. Electrical Distribution Report (part of PPAP).
6. EMC Test Report (part of PPAP).
7. Joint Industry Standard Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices, IPC/JEDEC J-STD-020E, December 2014.

3. Appendices

3.1 Product info

#	Item	Description
1	Customer part number	
2	Supplier part number and data sheet	TJA1028TK/5V0/10, TJA1028TK/5V0/20, TJA1042TK/3, TJA1049TK, TJA1049TK/3, TJA1051TK/3
3	Device Description	TJA1028TK: LIN transceiver, combined with a low-drop, on-board voltage regulator. TJA1042TK/3, TJA1051TK/3: third generation high-speed CAN transceivers, providing an interface between CAN protocol controller and physical two-wire CAN bus; variant for direct interfacing to microcontrollers with supply voltages from 3 to 5 V. TJA1049TK: third generation high-speed CAN transceiver, providing an interface between CAN protocol controller and physical two-wire CAN bus. TJA1049TK/3: variant of TJA1049TK for direct interfacing to microcontrollers with supply voltages from 3 to 5 V.
4	Wafer / Die Fab Location & Process ID: a. Facility name / plant #: b. Street address: c. Country: d. Process ID: e. Facility name / plant #: f. Street address: g. Country: h. Process ID:	 SSMC 70 Pasir Ris Industrial Drive 1 Singapore ZM34_PA100TMX04 ICN8 Gerstweg 2, 6534AE Nijmegen The Netherlands PA100TMX04
5	Wafer Probe Location: a. Facility name / plant #: b. Street address: c. Country:	 NXP Manufacturing Thailand / ATBK 303 Moo 3 Chaengwattana Rd Laksi, Bangkok 10210 Thailand
6	Assembly Location & Process ID: a. Facility name / plant #: b. Street address: c. Country: d. Process ID: e. Facility name / plant #: f. Street address: g. Country: h. Process ID:	 NXP Manufacturing Thailand / ATBK 303 Moo 3 Chaengwattana Rd Laksi, Bangkok 10210 Thailand HVSON8 (SOT782-1) ASEN (current name: ATX-SZ) 188 Su Hong Xi Road, Suzhou Industrial Park, Suzhou China HVSON8 (SOT782-1)
7	Final Quality Control A (Test) Location: a. Facility name / plant #: b. Street address:	 NXP Manufacturing Thailand / ATBK 303 Moo 3 Chaengwattana Rd Laksi, Bangkok 10210

	c. Country: a. Facility name / plant #: b. Street address: c. Country:	Thailand ASEN (current name: ATX-SZ) 188 Su Hong Xi Road, Suzhou Industrial Park, Suzhou China
8	Wafer / Die: a. Wafer size: b. Die family: c. Die mask set revision & name: d: Die photo	 200mm TJA1028TK: LIN transceiver TJA1042TK/3: CAN transceiver TJA1049TK(/3): CAN transceiver TJA1051TK/3: CAN transceiver TJA1028TK: tf1433A (SSMC) / cf1433A (ICN8) TJA1042TK/3: tf1361D (SSMC) / cf1361D (ICN8) TJA1049TK(/3): tf1521A (SSMC) / cf1521A (ICN8) TJA1051TK/3: tf1371C (SSMC) / cf1371C (ICN8) See the PPAP's Certificate of Design, Construction, and Qualification (CDCQ)
9	Wafer / Die Technology Description: a. Wafer / Die process technology: b. Die channel length: c. Die gate length: d. Die supplier process ID (Mask #): e. Number of transistors or gates: f. Number of mask steps	 A-BCD3 1 µm 1 µm ZM34_PA100TMX04 (SSMC) / PA100TMX04 (ICN8) 19
10	Die Dimensions (excluding saw lane): a. Die width: b. Die length: c. Die height:	 TJA1028TK: 1.51 mm TJA1042TK/3: 1.41 mm TJA1049TK(/3): 1.41 mm TJA1051TK/3: 1.40 mm TJA1028TK: 2.16 mm TJA1042TK/3: 1.99 mm TJA1049TK(/3): 1.99 mm TJA1051TK/3: 1.84 mm 280 µm
11	Die Metallization: a. Die metallization material(s): b. Number of layers: c. Thickness (per layer): d. % of alloys (if present):	 TiTiN / AlCu (0.5%)/ TiN 3 M1: 600nm; M2: 600nm; M3: 900nm
12	Die Passivation: a. Number of passivation layers b. Die passivation material(s): c. Thickness(es):	 3 HDP Oxide / SRO / Silicon nitride 1.75 µm
13	Die Overcoat Material:	Wafer coating (Polyimide) 4 µm
14	Die cross-section of the basic structure	See Appendix A of the PPAP's Certificate of Design, Construction, and Qualification (CDCQ)
15	Die Prep Backside: a. Die prep method: b. Die metallization: c. Thickness(es):	 Chemical etched None n.a.

16	Die Separation Method: a. Kerf width (µm) b. Kerf depth (if not 100% saw): c. Saw method:	 n.a. Sawing
17	Die Attach: a. Die attach material ID: b. Die attach method: c. Die placement diagram:	 QMI519 Glue See Appendix B of the PPAP's Certificate of Design, Construction, and Qualification (CDCQ)
18	Package: a. Type of package: b. Ball / lead count: c. JEDEC designation: d. Lead (Pb) free: e. Package outline drawing:	 Surface Mount Device 8 Pins MO-229 Yes cf. datasheet
19	Mold Compound: A Mold compound supplier ID: b. Mold compound type: c. Flammability rating: d. Fire retardant type / composition: e. Tg (glass transition temperature) (°C): f. CTE (above & below Tg) (ppm/ °C):	 Hitachi CEL-9220 UL-94-VO-1/8 120 CTE1 (below Tg) = 8, CTE2 (above Tg) = 33
20	Wire Bond: a. Wire bond material: b. Wire bond diameter: c. Type of wire bond at die: d. Type of wire bond at leadframe: e. Wire bonding diagram:	 AuPd 18 µm Ball bond Stitch bond See Appendix B of the PPAP's Certificate of Design, Construction, and Qualification (CDCQ)
21	Lead frame a. Paddle / flag material: b. Paddle / flag width: c. Paddle / flag length: d. Paddle / flag plating composition: e. Paddle / flag plating thickness: f. Leadframe material: g. Leadframe bonding plating composition: h. Leadframe bonding plating thickness: i. External lead plating composition: j. External lead plating thickness:	 CuFe2P 1.94 mm (TJA1028TK) / 1.90 [TJA1042TK/3, TJA1049TK(/3), TJA1051TK/3] 2.70 mm (TJA1028TK) / 2.50 [TJA1042TK/3, TJA1049TK(/3), TJA1051TK/3] NiPdAuAg, roughened Ni 0.5 µm, Pd 0.005 µm, Au 0.005 µm, Ag 0.005 µm CuFe2P NiPdAuAg Ni 0.5 µm, Pd 0.005 µm, Au 0.005 µm, Ag 0.005 µm NiPdAuAg Ni 0.5 µm, Pd 0.005 µm, Au 0.005 µm, Ag 0.005 µm
22	Substrate: (if applicable): a. Substrate material (e.g., FR5, BT, etc.): b. Substrate thickness (mm): c. Number of substrate metal layers: d. Plating composition of ball solderable surface: e. Panel singulation method: f. Solder ball composition: g. Solder ball diameter (mm):	Not applicable

23	Unpackaged Die:	Not applicable
24	Header Material:	Not applicable
25	Derived value of $\theta_{JA:}$	50 K/W (in free air, 2S2P board)
26	Test circuits, bias levels & operational conditions imposed during the supplier's life and environmental tests:	See appendices C and D of the PPAP's Certificate of Design, Construction, and Qualification (CDCQ)
27	Fault Grade Coverage:	>99 %
28	Maximum Process Exposure Conditions	SnPb: MSL1 @ 240°C (max dwell time:20 s) Pb free: MSL1 @ 260°C (max dwell time:30 s)

3.2 Application mission profile

The mission profile listed in Table 9 has been used to assess suitability of the product types for their intended application. This mission profile is the collection of relevant environmental and functional loads that the product types will be exposed to during their lifetime.

Table 9. Mission Profile

Mission Profile 'Automotive' (covering AEC Q100 grade 1)

Operation						Field Lifetime =	15	Years
Field Lifetime	Power-On-Hours (POH)		Relevant Temperatures		Stimuli	Power On Hours =	2.2	hours/day
						cycles/day =	2	cycles/day
years	hours/day	hours/field life	$T_{j,max-eff}$	T_a	(V, I, f, loading)	$T_{a,max-eff}$ =	84 °C	
15 years	2.2 h	12000 h	109 °C	-40 to 125 °C	Application Specific	ΔT_{self} =	25 °C	
Thermo Mechanical Loading						$T_{j,max-eff}$ =	109 °C	
Field Lifetime	Power Cycles		Relevant Temperatures		Effective Temperature Cycle	T_a =	-40 to 125	°C
years	cycles/day	cycles/field life	$T_{j,max-eff}$	$T_{e,min-eff}$	ΔT_{eff}	$T_{e,min-eff}$ = (TC / BL TC)	-3 °C	4 °C
15 years	2 c	10950 c	109 °C	-3 °C	112 °C	$T_{trop,day}$ =	30 °C	
Humid Environment						$T_{trop,night}$ =	15 °C	
Field Lifetime	Time Standby (with bias)		Relevant Temperatures		Relative Humidity	Relative humidity =	95%	
years	hours/day	hours/field life	$T_{trop,day}$	$T_{trop,night}$		$T_{solderjoint,max-eff}$ =	109 °C	
15 years	21.8 h	119400 h	30 °C	15 °C	95%			
Hot Environment								
Field Lifetime	POH + Time Standby + Time Off		Relevant Temperatures					
years	hours/day	hours/field life	$T_{j,max-eff}$	$T_{trop,day}$				
15 years	2.2 + 21.8 + 0 h	131400 h	109 °C	30 °C				

Based on the mission profile, the stress test read points for the relevant reliability tests have been defined, see Table 10.

Table 10. Stress test conditions and read-points.

Test	Condition		Based on mission profile	Standard read point	Robust read point
HTOL	150 °C		1519 h	1000 h	2000 h
HTSL	175 °C		223 h	500 h	1000 h
TC	-65 °C	150 °C	798 c	500 c	1000 c
THB	85 °C	85%	1640 h	1000 h	2000 h
BL TC	-40 °C	125 °C	4256 c	1500 c	3500 c

3.3 Qualification by similarity

Tables 11 - 15 show the relevant product parameters that were considered in the qualification by similarity assessment for MSLA, TC, HAST, HTSL, and BL-TC, respectively. The cells with yellow fill color indicate the parameters that were key in selecting the lead vehicles.

Table 11. MSLA structural similarity

	More critical if		Product to be qualified	Product to be qualified	Product to be qualified	Product to be qualified
Product type name/version			TJA1028TK	TJA1042TK/3	TJA1049TK(/3)	TJA1051TK/3
Die size in mm	N/A		2.16 x 1.51	1.99 x 1.41	1.99 x 1.41	1.84 x 1.40
Body size in mm	Larger		3 x 3 x 0.85 SOT782-1	3 x 3 x 0.85 SOT782-1	3 x 3 x 0.85 SOT782-1	3 x 3 x 0.85 SOT782-1
Tpeak Reflow	Higher		260C	260C	260C	260C
Total body thickness in mm	Larger		0.85	0.85	0.85	0.85
Thickness MC die top to body top	Larger		0.37	0.37	0.37	0.37
Asymmetry of package MC thickness under die pad in mm	Larger		exposed die pad	exposed die pad	exposed die pad	exposed die pad
Die pad size in mm (diagonal)	Larger, as long as die/die-pad ratio is the same within 15%		3.32	3.14	3.14	3.14
Die - die pad ratio in % (diagonal)			81%	80%	80%	76%
Length of lead within package in mm	Larger		0.4	0.4	0.4	0.4
Wire length (in µm)	Smaller		758 max	989 max	989 max	989 max
Wire length embedded in Chipcoat	Shorter		N.A.	N.A.	N.A.	N.A.
Die free surface area (for stacked dies)	Larger		N.A.	N.A.	N.A.	N.A.

Table 12. TC structural similarity

	More critical if		Product to be qualified	Product to be qualified	Product to be qualified	Product to be qualified
Product type name/version			TJA1028TK	TJA1042TK/3	TJA1049TK(/3)	TJA1051TK/3
die size in mm	N/A		2.16 x 1.51	1.99 x 1.41	1.99 x 1.41	1.84 x 1.40
Damage response after MSLA	Worse		Equal	Equal	Equal	Equal
Total body thickness in mm	Larger		0.85	0.85	0.85	0.85
Thickness MC die top to body top	Larger		0.37	0.37	0.37	0.37
Asymmetry of the subpackage MC below the die pad	Larger		N.A.	N.A.	N.A.	N.A.
Die pad size in mm (diagonal)	Larger as long as die/die-pad ratio is the same within 15%		3.32	3.14	3.14	3.14
Die - die pad ratio in % (diagonal)			81%	80%	80%	76%
Wire length (in µm)	shall be equal or smaller		758 max	989 max	989 max	989 max
Wire diameter	shall be equal or smaller		18 µm	18 µm	18 µm	18 µm
Solder Ball diameter	shall be equal or smaller		N.A.	N.A.	N.A.	N.A.
Wire length embedded in Chipcoat	shall be equal or shorter		N.A.	N.A.	N.A.	N.A.
Overhang of the top die	shall be equal or larger		N.A.	N.A.	N.A.	N.A.

Table 13. HAST structural similarity

	More critical if		Product to be qualified	Product to be qualified	Product to be qualified	Product to be qualified	Product to be qualified
Product type name/version			TJA1028TK	TJA1042TK/3	TJA1049TK	TJA1049TK/3	TJA1051TK/3
Damage response after MSLA	Worse		Equal	Equal	Equal	Equal	Equal
Thickness MC die top to body top	Smaller		0.37	0.37	0.37	0.37	0.37
Applied E-field Between any metal parts if pass data extends to 2x the required readpoint, the applied E-field of the reference can be 50% smaller.	Larger		28V / 0.15mm 187 V/mm	5V / 0.15mm 33 V/mm	5V / 0.15mm 33 V/mm	5V / 0.15mm 33 V/mm	5V / 0.15mm 33 V/mm

Table 14. HTSL structural similarity

	More critical if		Product to be qualified	Product to be qualified	Product to be qualified	Product to be qualified	Product to be qualified
Product type name/version			TJA1028TK	TJA1042TK/3	TJA1049TK	TJA1049TK/3	TJA1051TK/3
Wire diameter	Smaller		18 µm	18 µm	18 µm	18 µm	18 µm

Table 15. BL-TC structural similarity

	More critical if		Product to be qualified	Product to be qualified	Product to be qualified	Product to be qualified
Product type name/version			TJA1028TK	TJA1042TK/3	TJA1049TK(/3)	TJA1051TK/3
Body size in mm	Larger		3.0 x 3.0	3.0 x 3.0	3.0 x 3.0	3.0 x 3.0
Solder volume	Smaller		equal	equal	equal	equal
Pitch in mm	Not equal		0.65	0.65	0.65	0.65
Die size in mm	Larger		2.16 x 1.51	1.99 x 1.41	1.99 x 1.41	1.84 x 1.40
Array size / pin count	Larger		8	8	8	8

3.4 Final test at read-points

The final-test temperatures applied at the various read-points of the reliability and electrical robustness tests are listed in Table 16.

Table 16. Final-test temperatures at read points[3]

Test	Abbr.	Cold (-40 ºC)	Room (25 ºC)	Hot (125 ºC)[3]
Electrical Distribution	ED	X	X	X
ESD Human Body Model	HBM		X	X
ESD Charged Device Model	CDM		X	X
Early Life Failure Rate	ELFR		X	X
High Temperature Operating Life	HTOL	X	X	X
High Temperature Storage Life	HTSL		X	X
Highly Accelerated Stress Test	HAST	X	X	X
Temperature Cycling	TC	X	X	X

Parameter shift analyses were performed after HTOL, HBM, and CDM (up to spec level and one level above).

[3] Table also covers final testing after preconditioning prior to HAST and TC tests.

3.5 Wire bond shear

The 0-hrs wire ball shear results are shown in Table 17.

Table 17. 0-hrs Wire bond shear results (post seal)

	QB1	QB3	QB4	QB5	QB6	QB7	QB8	QB9	QB10	QB11	QB12	QB13	QB14	QB15		
Parameter	**New stress test results – generated on the product type(s) to be qualified**														**Generic data – previously generated on the current product type(s)**	
Qual Lot ID	Lot 1	Lot 4	Lot 5	Lot 7	Lot 8	Lot 9	Lot 10	Lot 11	Lot 12	Lot 13	Lot 14	Lot 15	Lot 16	Lot 17	Lot 25	Lot 23
Ball Shear Average [g]	26.65	25.73	27.10	26.93	24.28	23.79	24.94	25.39	24.65	25.44	24.57	26.20	25.18	24.51	39.26	25.85
Highest Reading [g]	29.26	34.36	28.93	28.54	27.08	25.34	28.61	27.94	28.11	27.12	27.43	28.02	27.93	28.02	42.71	29.19
Lowest Reading [g]	24.71	22.73	23.68	25.67	22.81	21.79	22.98	23.32	21.63	23.25	20.34	23.72	22.01	21.44	35.21	21.88
Standard deviation	0.92	1.96	0.99	0.66	0.86	0.83	1.09	0.99	1.28	0.98	1.45	0.86	1.38	1.45	1.7	1.71
Sample size [#wires from #samples]	50 wires from 5 samples	55 wires from 5 samples	50 wires from 5 samples	55 wires from 5 samples	50 wires from 5 samples	50 wires from 5 samples	55 wires from 5 samples	60 wires from 5 samples	55 wires from 5 samples	60 wires from 5 samples	55 wires from 5 samples	60 wires from 5 samples	55 wires from 5 samples	60 wires from 5 samples	50 wires from 5 samples	55 wires from 5 samples
Failure Mode:																
Bond Shear / Al Shear	98%	100%	86%	100%	100%	94%	100%	93%	100%	100%	43%	92%	55%	15%	100%	62%
Metal Peel Off	2%	0%	8%	0%	0%	6%	0%	7%	0%	0%	57%	8%	46%	85%	0%	27%
Cratering/COUB	0%	0%	6%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0	0
Avg. Ball Bond diameter in µm	50	53	47	53	50	52	49	50	50	48	51	49	50	50	61	
AEC-Q100 specified Minimum Sample Average [g]	18	20	21	20	18	20	16	18	18	16	18	16	18	18	18.8	12
AEC-Q100 Minimum individual Shear Reading [g]	12	14	10	14	12	14	11	12	12	11	12	11	12	12	10.9	
Ppk (>1.67)	5.31	1.99	5.76	6.52	4.77	3.95	4.26	4.51	3.29	4.91	2.89	5.89	3.18	2.88	5.57	2.7
Conclusion against AEC-Q100 requirements	Pass	Pass	Fail [a]	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass

Notes:

a. Cratering was observed as failure mode during ball-shear test. This problem has been addressed and resolved, see section 2.3.1.

3.6 Wire bond pull 0 hrs

The 0-hrs wire bond pull results are shown in Table 18.

Table 18. 0-hrs Wire bond pull results (post seal)

	QB1	QB3	QB4	QB5	QB6	QB7	QB8	QB9	QB10	QB11	QB12	QB13	QB14	QB15		
Parameter	**New stress test results – generated on the product type(s) to be qualified**														**Generic data – previously generated on the current product type(s)**	
Qual Lot ID	Lot 1	Lot 4	Lot 5	Lot 7	Lot 8	Lot 9	Lot 10	Lot 11	Lot 12	Lot 13	Lot 14	Lot 15	Lot 16	Lot 17	Lot 25	Lot 23
Bond Pull Average [g]	6.88	6.73	7.29	7.39	7.70	7.11	7.66	7.57	7.77	7.39	7.81	7.58	7.68	7.62	9.3	7.47
Highest Reading [g]	7.87	8.36	8.29	9.04	8.97	7.59	9.40	9.54	9.54	9.04	8.70	8.39	8.57	8.54	10.09	8.83
Lowest Reading [g]	5.43	4.08	6.60	5.23	6.49	6.64	5.00	6.10	6.29	5.23	6.81	6.36	6.35	6.10	8.46	5.54
Standard deviation	0.53	0.87	0.38	0.96	0.53	0.22	0.84	0.79	0.70	0.96	0.47	0.49	0.45	0.56	0.36	0.83
Sample size [#wires from #samples]	50 wires from 5 samples	55 wires from 5 samples	50 wires from 5 samples	55 wires from 5 samples	50 wires from 5 samples	50 wires from 5 samples	55 wires from 5 samples	60 wires from 5 samples	55 wires from 5 samples	60 wires from 5 samples	55 wires from 5 samples	60 wires from 5 samples	55 wires from 5 samples	60 wires from 5 samples	50 wires from 5 samples	55 wires from 5 samples
Failure Mode:																
Break on intermetallic	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
Ballneck break	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
Wire fracture	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
AEC-Q100 specified Minimum [g]	≥ 2.0															
Ppk (>1.67)	3.05	1.82	4.68	1.87	3.56	7.63	2.25	2.35	2.75	1.87	4.12	3.80	4.21	3.35	7.02	2.1
Conclusion against AEC-Q100 requirements	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass

3.7 Wire bond pull after TC 500 cls

The wire bond pull results after TC 500 cycles are shown in Table 19.

Table 19. TC 500-cls Wire bond pull results (post seal)

Parameter	New stress test results – generated on the product type(s) to be qualified			Generic data – previously generated on the current product type(s)
Qual Lot ID	Lot 1	Lot 3	Lot 5	Lot 17
Bond Pull Average [g]	7.17	7.33	7.42	9.34
Highest Reading [g]	8.83	8.31	8.87	10.73
Lowest Reading [g]	5.27	6.62	6.22	8.69
Standard deviation	0.65	0.45	0.59	0.47
Sample size [#wires from #samples]	50 wires from 5 samples	50 wires from 5 samples	50 wires from 5 samples	50 wires from 5 samples
Failure Mode:				
Break on intermetallic	0%	0%	0%	0
Ballneck break	100%	100%	100%	1
Wire fracture	0%	0%	0%	0
AEC-Q100 specified Minimum [g]	≥ 2.0			
Ppk (>1.67)	2.65	3.97	3.05	5.32
Conclusion against AEC-Q100 requirements	Pass	Pass	Pass	Pass

3.8 Solderability

The solderability results for are shown in Table 20. The solder reflow is defined according to the guidelines for Pb-free assembly in IPC/JEDEC J-STD-020E [7].

Table 20. Solderability results

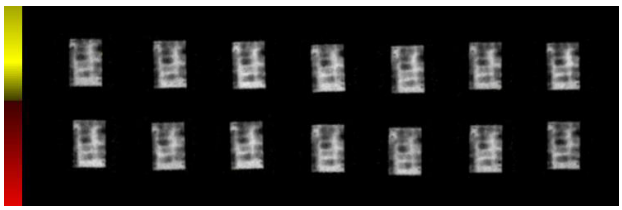
Parameter	New stress test results – generated on the product type(s) to be qualified
Qual Lot ID	Lot 1
Method	SMT
Profile	NXP
Precondition	**Steam aging 1 hour**
SnPb Profile	15 / 15
Pb-Free Profile	15 / 15
Precondition	**Dry bake 150 °C 16 hours**
SnPb Profile	15 / 15
Pb-Free Profile	15 / 15
Visual Inspection	
Solder Defects	None
Solder Coverage	Acceptable

3.9 Solder ball shear

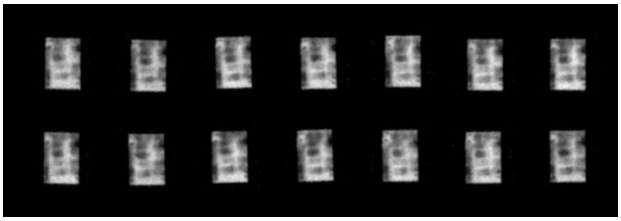
Solder ball shear testing is not applicable, because the device's package does not include solder balls.

3.10 CSAM

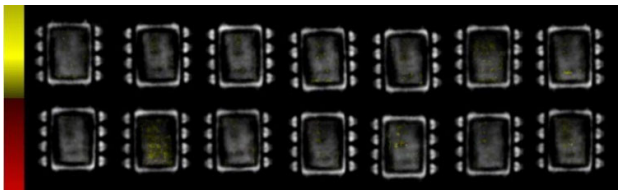
The images shown in Figure 3 show the CSAM results of lot 1 that have been collected during moisture sensitivity level assessment (MSLA). No delamination was observed, neither at 0 hrs nor after MSL1 test. The images refer to lot 1 manufactured in SSMC and assembled in ASEN, but are also representative for other analyzed lots, including those manufactured in ICN8 and/or assembled in ATBK.



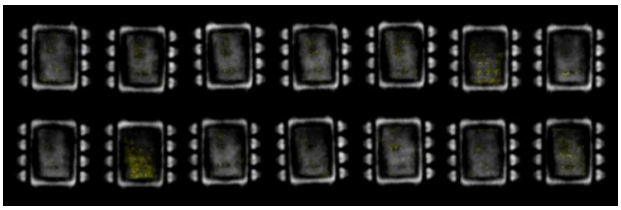
a) C-Scan (top-side) at 0 hrs (focus on die)



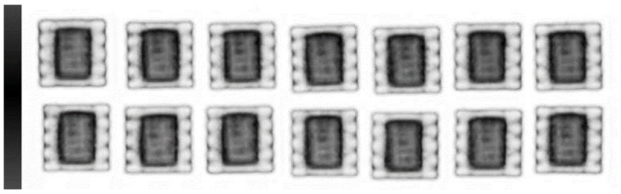
b) C-Scan (top-side) after MSL1 test (focus on die)



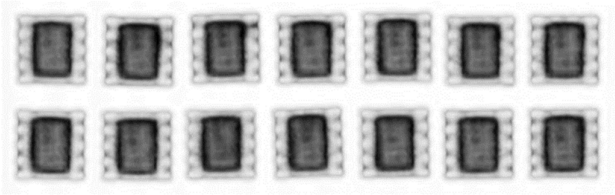
c) C-Scan (top-side) at 0 hrs (focus on die-pad and leads)



d) C-Scan (top-side) after MSL1 test (focus on die-pad and leads)



e) Through-Scan at 0 hrs



f) Through-Scan after MSL1 test

Figure 3. CSAM results.

After PCON of lot 5, lead delamination was observed, see Figure 4. This issue is discussed in section 2.3.2.

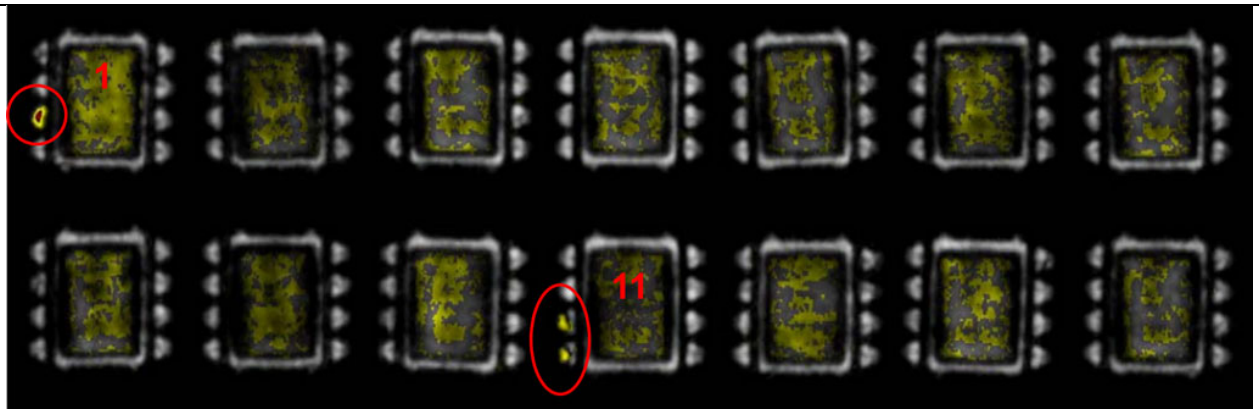


Figure 4. Lead delamination observed after PCON before HAST for lot 5.

3.11 XRAY

Figure 5 shows an X-ray image of a qualification sample, illustrating lead-frame design, internal package structure, and wiring. The images refer to lot 1 manufactured in SSMC and assembled in ASEN, but are also representative for other analyzed lots, including those manufactured in ICN8 and/or assembled in ATBK.

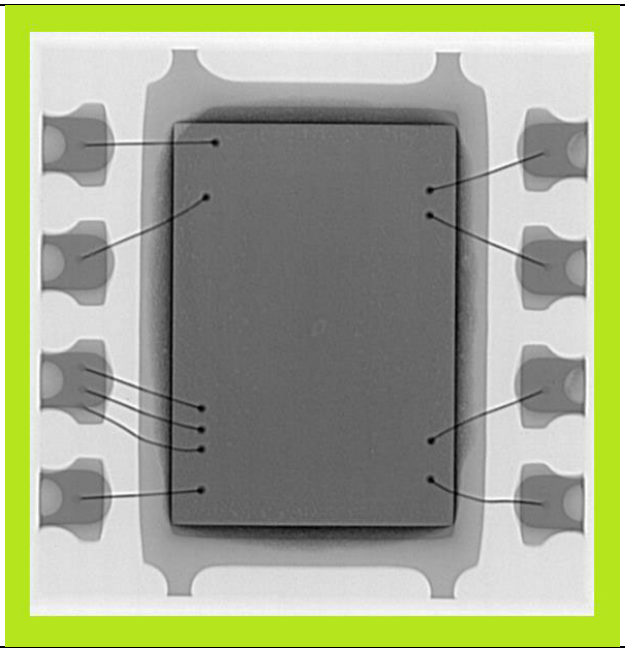


Figure 5. X-ray photo.

3.12 Wire-diameter change (20 to 18 μm) at ATBK

With the quadruple-source release, a wire-diameter change from 20 to 18 μm is introduced for TJA1028TK, TJA1042TK/3, and TJA1051TK/3 in HVSON8 (SOT782-1) at ATBK. The risk of the wire diameter change is very low, because multiple other product types from PL IVN (TJA1044TK, TJA1044TK/3, TJA1057TK, TJA1057TK/3) manufactured in wafer fabs ICN8 and SSMC have already been released with 18-μm wire diameter at ATBK and are running in volume production.

TJA1028TK, TJA1042TK/3, and TJA1051TK/3 with 20-μm wire diameter are fully structural similar to the same product type assembled with 18-μm wire diameter for accelerated environment stress tests (test group A). The 0-hrs performance specifically related to the wire-diameter change and, therefore, to the wire-bonding process have been experimentally verified, for dies manufactured both in ICN8 and in SSMC wafer fabrication sites. The construction analysis results are listed in Table 5.

Additionally, CDM testing was performed, for both ICN8 and SSMC dies. The CDM results are listed in Table 7.